The opinion in support of the decision being entered today is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROBERT F. CANNATA and JEFFREY L. METSCHULEIT

Appeal 2006-1049
Application 09/667,826[1]
Technology Center 2800

Decided: December 28, 2006

Before: GARRIS, MCKELVEY, and MACDONALD, Administrative Patent Judges.

MACDONALD, Administrative Patent Judge.

REVERSED

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[1] Application filed September 21, 2000, seeking to reissue U.S. Patent 5,811,808, issued September 22, 1998, based on application 08/712,891, filed September 12, 1996. The real party in interest is Raytheon Systems Company (Brief at page 1).

DECISION ON APPEAL UNDER 35 U.S.C. § 134

The Examiner has rejected claims 1, 5, 21, 22, 40, 42, and 48 of the reissue application on appeal under 35 U.S.C. § 102(b) as being anticipated.

The Examiner has rejected claims 6, 7, 12, 13, 15, 19, 24, 25, 44-47, and 50 of the reissue application on appeal under 35 U.S.C. § 103(a) as being obvious.

The Examiner has rejected claims 40-50 and 52-58 of the reissue application on appeal as being unpatentable under 35 U.S.C. § 251 based on recapture.

The Examiner has rejected claims 40-50 and 52-58 of the reissue application on appeal under 35 U.S.C. § 112, first paragraph, as failing to meet the written description requirement.

With respect to the rejections under 35 U.S.C. §§ 102(b), 103(a), § 112, and § 251, the panel reverses the decision of the Examiner.

DECISION ON APPEAL

I. INTRODUCTION

1. Applicants appeal from a final rejection entered January 17, 2002.

2. The reissue application on appeal seeks to reissue U.S. Patent 5,811,808, issued September 22, 1998, based on application 08/712,891, filed September 12, 1996.

3. The reissue application contains claims 1-35 and 40-58.

4. Claims 40-50 and 52-58 have been rejected under 35 U.S.C. § 251 on the grounds that these claims seek to recapture subject matter surrendered when the patent sought to be reissued was granted.

5. Claims 40-50 and 52-58 have been rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

6. Claims 1, 5, 21, 22, 40, 42, and 48 have been rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent 4,752,694, to Hegel, Jr. et al (Hegel).

7. Claims 6, 7, 12, 13, 15, 19, 24, 25, 44-47, and 50 have been rejected under 35 U.S.C. § 103(a) on the grounds that these claims are unpatentable over Hegel.

8. An objection has been made to claim 51.[2]

9. Claims 2-4, 8-11, 14, 16-18, 20, 23, and 26-35 have been indicated as being allowable.

10. Appellants filed:

(1) an Amended Appeal Brief (the brief) on August 26, 2002, fully replacing an Appeal Brief filed June 19, 2002;

(2) a Reply Brief (the reply) on January 3, 2003; and

(3) a Supplemental Reply Brief (the supplemental reply) on March 4, 2005.

11. The first issue before the Board is whether Appellants have established that the Examiner erred in rejecting claims 40-50 and 52-58 under 35 U.S.C. § 251 based on recapture.

[2] Appellants request the Board to order the Examiner to enter the after final amendment filed March 5, 2002 (Brief at page 4). We do not review issues associated with an examiner's decision not to enter an amendment. In any event, the request is moot as Applicants may now request entry before the Examiner based on the result reach herein.

12. The second issue before the Board is whether Appellants have established that the Examiner erred in rejecting claims 40-50 and 52-58 under 35 U.S.C. § 112, first paragraph.

13. The third issue before the Board is whether Appellants have established that the Examiner erred in rejecting claims 1, 5, 21, 22, 40, 42, and 48 under 35 U.S.C. § 102(b).

14. The fourth issue before the Board is whether Appellants have established that the Examiner erred in rejecting claims 6, 7, 12, 13, 15, 19, 24, 25, 44-47, and 50 under 35 U.S.C. § 103(a).

II. FINDINGS OF FACT

The following findings of fact are believed to be supported by a preponderance of the evidence.

A. *The Invention*

1. This invention relates to infrared detection systems and imaging systems. More particularly, the present invention relates to infrared detection and

imaging systems employing either non-cooled or cryogenically cooled focal plane arrays. (U.S. Patent 5,811,808, col. 1, lines 7-11).

2. Applicants state at column 2, lines 5-8, that:

> A consideration which is extremely important for maximizing the quality of the output image from a focal plane array infrared detector is compensating for nonuniformity in the individual detector elements in the array.

3. Applicants further state at column 2, lines 8-17, that:

> Whereas ideally a uniform temperature scene directed to the focal plane array would produce a completely uniform output at each pixel, in practice, the output of the individual detector elements may vary by a significant percentage of the average output level. When an actual scene is detected, such detector element nonuniformity can significantly degrade the image quality or even completely mask the actual image. This degrading of the image due to detector element nonuniformity is sometimes called spatial or fixed pattern noise.

4. Applicants opine at column 2, lines 33-42, that:

> The problem of nonuniformity in the detector elements is directly related to issues of manufacturing throughput and cost. That is, if very high uniformity is required for the detector arrays to ensure good image quality, the number of focal plane arrays which must be rejected will increase on average. This in turn reduces throughput, increasing per unit costs. Therefore, it is generally preferable for nonuniformity to be tolerated by virtue of compensation in the detector electronics rather than controlling nonuniformity during detector array fabrication.

5. Applicants state at column 3, lines 18-33, that:

> The present invention provides a solution to the above noted problems by providing an infrared focal plane array detection system employing on-focal plane nonuniformity correction which compensates for the inherent nonuniformities in the detector elements forming the focal plane array. This allows nonuniformities in the detection signal outputs from the individual detector elements in the focal plane array to be compensated prior to the amplification necessary for further signal processing. This in turn provides improved image quality as well as reduced cost in the signal processing circuitry by avoiding the necessity for expensive high resolution analog-to-digital converters and associated digital offset correction processing. Additionally, greater nonuniformities in detector arrays may be tolerated increasing yields, and hence reducing cost, of an array manufacturing process.

6. The invention can be understood by reference to Figures 1, 2, 3A, 3B, 7, and 10 of the drawings, all of which are reproduced in Appendix 1 of this opinion.

7. Referring to Figure 1, a block schematic drawing of an infrared focal plane array imaging system in accordance with the present invention is illustrated. (col. 4, lines 65-67).

8. As shown, the principal components of the infrared imaging system include focal plane array 10, detector array interface circuit 12, focal plane sensor controller 14, and display processor 16. Incident infrared (IR) radiation is focused onto the focal plane array 10 via IR lens 18 (col. 5, lines 1-5).

9. The focal plane array 10 preferably employs an array of detector elements formed in a two dimensional array, corresponding to the pixels of the image data (col. 5, lines 11-13).

10. Focal plane array 10 may preferably employ an array of microbolometer detector elements formed directly on a readout circuit IC acting as a substrate, to form the combined detector/readout structure (col. 5, lines 17-20).

11. The focal plane array 10 will preferably be configured on a support, such as a ceramic substrate configured inside a vacuum chamber. Also, a thermoelectric cooler is preferably provided (not shown) to stabilize the temperature of the readout substrate (col. 5, lines 41-45).

12. The output of focal plane array 10, which provides the detection signals corresponding to each pixel of the array, is provided on one or more output lines 20. The output signals are preferably time multiplexed to reduce the number of pins required (col. 6, lines 1-5).

13. The electrical inputs to focal plane array 10 in turn are biasing signals needed to bias the detector elements and drive the readout circuit and timing signals to control the readout of signals from the array (col. 6, lines 5-8).

14. These timing signals and electrical biasing signal inputs are illustrated by lines 22 and 25, respectively, in Figure 1 (col. 6, lines 10-12).

15. Focal plane array 10 also receives digital offset correction signals provided along line 23 which allow individual correction of offsets due to nonuniformities in each detector element of the array (col. 6, lines 12-15).

16. The focal plane sensor controller 14, as its name suggests, provides intelligent control of the focal plane array 10. In particular, during initial calibration of the focal plane array and optional subsequent calibrations, the uniformity in the individual detector elements in the focal plane array 10 is detected and digital offset correction coefficients stored in offset coefficient memory 26 (col. 6, line 66 through col. 7, line 5).

17. Uniformity offset coefficients are thus provided in parallel form along lines 34 to detector array interface circuit 12, which provides the coefficients along lines 23 to the focal plane array 10, in synchronism with the appropriate timing signals to control readout and simultaneous offset correction (col. 7, lines 37-43).

18. Figures 2 and 3A, 3B and 3C, describe in more detail the readout circuitry of the focal plane array 10 in accordance with the present invention.

Figure 2 illustrates a focal plane array 10 of pixels arranged into an array of M columns and N rows (col. 8, lines 63-67).

19. The focal plane array 10 of Figure 2 operates as follows (col. 8, line 67 through col. 9, line 17):

> The readout circuit includes a plurality of readout cells 100, MxN in number, corresponding to each pixel. The individual readout cells illustrated in FIG. 2 are read out by a plurality of column and row address lines 102, 104, respectively. Thus, as illustrated, a plurality of column address lines 102 provide respective column select (CS) signals CS_1, CS_2 . . . CS_M, corresponding to each column of the MxN array, to corresponding switches 110. Similarly, a plurality of row address lines 104 provide respective row select (RS) signals RS_1, RS_2 . . . RS_N corresponding to the N rows of the MxN focal plane array to row select switches 112. The column select and row select signals are strobed so as to read out the individual readout cells 100 in a desired manner, for example, in a raster scan row-by-row readout pattern or any other desired readout sequence. The output from each readout cell 100 is thus provided in a time multiplexed manner to serial output line 20 illustrated in FIG. 1.

20. The readout of the individual readout cells 100 may preferably be provided in a multiplexed manner. For example, as illustrated, the readout cells 100 may be multiplexed through output multiplexer (MUX) logic 120 and associated output buffers 106 and output switches 122. The output MUX logic 120 in turn receives the focal plane array timing signals 22, and generates output

multiplex control signals $SELECT_1$, $SELECT_2$ . . . $SELECT_M$ which are provided to respective output switches 122 (col. 9, lines 37-46).

21. Still referring to FIG. 2, compensation for nonuniformities in the detector elements in each pixel can be achieved by offset correction circuitry in each readout cell 100, described below, controlled by offset correction logic 130 (col. 10, lines 3-6).

22. Additionally, the offset correction control logic 130 may provide an optional timing signal RST illustrated as being provided along line 140, for use in the optional embodiment described below in relation to FIG. 3B (col. 10, lines 27-30).

23. Referring to FIGS. 3A and 3B, the readout cell circuitry corresponding to an individual readout cell 100 of FIG. 2 is illustrated in an implementation employing microbolometer detector elements. More specifically, FIG. 3A illustrates a readout cell employing a preferred approach to biasing of a microbolometer detector element while FIG. 3B illustrates the readout cell of FIG. 3A further including a nonuniformity correction circuit, in accordance with the present invention (col. 11, lines 19-27).

24. Referring first to FIG. 3A an individual readout cell 100 is illustrated incorporating therein a microbolometer detector element 200. A microbolometer detector is simply a temperature sensitive resistor which changes its resistance in relation to the IR energy illuminating the detector, which IR energy raises or lowers the temperature of the detector (col. 11, lines 29-35).

25. Sensing the detector resistance (illustrated in FIG. 3A by R_D) across microbolometer 200, allows the incident IR energy on the detector element to be detected. This change in resistivity must be sensed by some signal, which in turn, requires biasing the detector 200 so as to get an output signal which varies with the resistance of R_D (col. 11, lines 35-41).

26. More specifically, referring to FIG. 3A, the readout cell circuitry includes a constant current source 202 which provides the bias current I_{bias} (col. 12, lines 22-24).

27. Although the constant current source 202 is shown as coupled directly to the positive voltage source V_+ in FIG. 3A, as better illustrated in FIG. 2, the readout cell is coupled to the voltage source via a column select switch 110 which will only be activated when readout of the particular column in which the readout cell 100 resides is desired (col. 12, lines 27-32).

28. An additional column select switch 203 optionally may be provided within readout cell 100 (col. 12, lines 32-34).

29. A row select switch 204 is also provided, which receives the row select signal (RS) which is activated when readout of the specific row corresponding to the readout cell 100 is desired (col. 12, lines 34-37).

30. When the appropriate column select and row select strobes are presented, the constant current source 202 will be connected to the microbolometer element 200 and the row select switch 204 will be closed so that a voltage appears at node 206 corresponding to the voltage drop V_D across the microbolometer element (col. 12, lines 38-43).

31. A short time after the closing of the column select and row select switches corresponding to the specific readout cell 100 are completed, sufficient to give time for the detector sample voltage V_D to stabilize, the control signal SAMPLE is applied to sampling switch 208 (col. 12, lines 43-47).

32. The closure of switch 208 causes a voltage to appear at node 210 which, given sufficient time to settle, will correspond to the sampled value of the microbolometer voltage V_D (col. 12, lines 48-50).

33. A sample and hold capacitor 212 is then charged to the sample value of the microbolometer voltage V_D. This held voltage is then provided as the output of the readout cell indicated as V_{out} on line 214 in FIG. 3A (col. 12, lines 55-59).

34. Referring to FIG. 3B, the readout cell 100 is illustrated employing offset correction circuitry for compensating for nonuniformities in the detector elements in the array of FIG. 2. The readout circuitry of FIG. 3B common to that of FIG. 3A operates in the manner described above and a detected voltage V_D is provided at node 210 as described above (col. 12, lines 60-65).

35. Applicants state that voltage V_D will vary from pixel to pixel even for a uniform scene and uniform IR input to all the microbolometer elements 200 due to inherent nonuniformities in processing of the microbolometer array (col. 12, line 66 through col. 13, line 2).

36. In the present invention, such nonuniformities are compensated for by offset correction circuit 220 which is coupled to node 222 and causes a suitable amount of charge to be subtracted from (or added to) sample and hold capacitor 212 such that an offset corrected output voltage V_{out} is provided. That is, the offset correction circuit 220 provides a corrected output voltage V_{out} at node 222 (col. 13, lines 2-8).

37. In a preferred implementation, as illustrated in FIG. 3B, the offset correction circuit 220 includes a plurality of parallel coupled capacitors 224. Capacitors 224 are coupled between output node 222 and a reference node 226 maintained at an offset reference voltage V_R, via respective switches 228 (col. 13, lines 13-18).

38. Switches 228 receive the binary offset correction coefficients S_0-S_N described above to select the specific capacitors 224 which are coupled into the offset correction circuit 220 (col. 13, lines 18-21).

39. Each capacitor 224 which is coupled to node 222 by virtue of the corresponding switch 228 being closed will subtract (or add) a voltage from (or to) node 222 corresponding to the difference between V_D and V_R and the capacitance of the capacitor 224 (col. 13, lines 21-25).

40. The respective capacitances of capacitors 224 are illustrated in FIG. 3B as C_0-C_N and are preferably chosen such that each capacitance is double that of the previous capacitor in the network; i.e. the capacitance of the Nth capacitor is $2^N C_0$. That is, the capacitors C_0-C_N have the following values:

$$C_0, 2C_0, 4C_0 \ldots 2^N C_0.$$

Thus, for example, for N=4, the offset compensation network will have 16 discrete

and uniform offset values corresponding to the binary value of the four offset coefficients S_0-S_N (col. 13, lines 25-37).

41. By adjusting these capacitance values as well as optionally the voltage V_R, the discrete step size of voltage correction corresponding to each capacitor which is switched into the network may be controlled (col. 13, lines 37-40).

42. In this way, a substantially uniform signal can be provided at V_{out} for each detector element when the detectors are uniformly illuminated, thereby correcting for nonuniformities in the individual detector elements 200 (col. 13, lines 40-44).

43. This stepwise correction of detector voltages to a uniform value for a uniform IR scene is illustrated in FIG. 7, discussed below (col. 13, lines 44-46).

44. As further shown in FIG. 3B (col. 13, lines 47-63):

> [T]he offset correction circuit 220 is coupled to the node 222 through switch 230 which is responsive to the signal OFFSET provided along line 136. The control signal offset maintains the OFFSET correction circuit 220 disconnected from node 222 until the sampled voltage V_D stabilizes at node 210 and the microbolometer detector is disconnected from node 210 by opening the sample switch 208. The signal OFFSET provided along line 136 then closes switch 230 to couple the offset correction network circuit 220 to node 222 and thereby subtract (or add) the desired charge from sample and hold capacitor 212 to provide the offset corrected voltage V_{out} along line 214. This offset switch 230 is momentarily closed and then opened to

> subtract (or add) charge from the sample and hold capacitor. It will be appreciated by those skilled in the art that the offset switch 230 is held closed a sufficient time to allow the voltage at node 222 to settle.

45. As still further shown in FIG. 3B (col. 13, line 64 through col. 14, line 6):

> [T]he offset correction circuit 220 receives control signal S-RST provided along line 134 to reset switch 232. Reset switch 232 serves to discharge (or precharge) capacitors 224 to the offset reference voltage V_R prior to coupling the offset correction circuit 220 to node 222. The reset is primarily necessary to remove any residual charge from capacitors 224 in situations where circuit 220 is shared between plural readout cells or to reset these capacitors and remove any residual charge from the previous sample of the detector voltage.

46. Referring to FIG. 7, the corresponding discrete offset corrections provided by 10 distinct offset correction coefficients for 10 consecutive pixels in a row of the focal plane array are illustrated (col. 16, lines 10-13).

47. Referring to FIG. 10, an alternate embodiment of the offset correction circuit 220 is illustrated, which employs a plurality of constant current sources 400 which are coupled in parallel and which are selectively connected to the node 222 (described above in relation to FIGS. 3B and 3C) by switches 228 (col. 16, lines 46-51).

48. As in the case of the embodiment described above in relation to FIGS. 3B and 3C, the switches 228 are selectively activated by the signals S_0-S_N which correspond to the stored offset correction coefficients (col. 16, lines 51-55).

B. *Prosecution history of the original application*

49. As noted earlier, the patent sought to be reissued was based on application 08/712,891, filed September 12, 1996 ("original application").

50. As filed, the original application contained claims 1-44 and 46-57, but no claim 45. Claims 46-58 were renumbered as original claims 45-57 (See 37 C.F.R. § 1.126). Claims 1-57 are reproduced in Appendix 2 of this opinion.

51. On March 7, 1997, the Examiner entered a Non-final Office action.

52. Claims 1, 5-7, 9-13, 21-23, 25-32, 38-44, and 46-57 were rejected on various grounds.

53. Claims 2-4, 8, 14-20, 24, 33-37, and 45 were "objected to" as being dependent on a rejected claim.

54. Claims 5, 6, 25-28, 48, and 50 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite.

55. Claims 1, 7, 10-11, 21, 23, 42-44, 46, 49-50, and 53-57 were rejected under 35 U.S.C. § 102 as being unpatentable over the following prior art:

(1) Lung, U.S. Patent 5,489,776.

56. Claims 9, 12-13, 22, 25, 29-32, 38-41, 47-48, and 51-52 were rejected under 35 U.S.C. § 103 as being unpatentable over Lung.

57. Claims 1, 5-6, 12, 21-22, 53, and 56 were rejected under 35 U.S.C. § 102 as being unpatentable over the following prior art:

(1) Masarik et al (Masarik), U.S. Patent 5,528,035.

58. Claims 9-10, 13, 25, 29-31, 41, 54-55, and 57 were rejected under 35 U.S.C. § 103 as being unpatentable over Masarik.

59. Lung and Masarik are prior art vis-à-vis applicant under 35 U.S.C. § 102(e).

60. The Examiner found that Lung and Masarik "anticipated" one or more of claims 1, 5-7, 10-12, 21-23, 42-44, 46, 49-50, and 53-57.

61. The Examiner held that given the description of Lung:

> It would have been obvious to facilitate assembly and maintenance by providing the detector array and readout circuit as a single monolithic integrated circuit. The use of output buffers would have depended on the intended applications. It would have been obvious to enhance versatility by providing means to adjust the reference voltage for the differential amplifiers. Use of a fixed voltage is conventional.

62. The Examiner further held that given the description of Lung:

> It would have been obvious to simplify assembly and maintenance by structurally integrating the detector elements and readout circuit. The Marsarik (sic) et al focal plane array uses pyroelectric detectors, but it would have been obvious that their techniques of offset correction would apply to other types of infrared detectors used in a focal plane array, with the type of readout circuit used being dependent on the type of detector. They amplify detector signals before correcting, but it would have been obvious that the amplification step could have been provided after the correction, with such being an obvious design choice.

63. The Examiner advised applicants that claims 2-4, 8, 14-20, 24, 33-37, and 45 would be allowable if written in independent form to include all the limitations of the claims from which they depend.

64. On September 9, 1997, applicants filed an amendment responding to the Examiner's first Office action.

65. As shown in Appendix 3 of this opinion, the amendment:

(1) cancelled claims 1, 23, 29-32, and 42-57; and

(2) amended claims 2, 5, 7, 9-10, 12-13, 21, 25-26, 33, 37-38, and claim 41. After entry of the amendment, the application claims were 2-22, 24-28, and 33-41.

66. In the amendment at page 9, applicants stated as follows:

> The Examiner indicated that claims 2-4, 8, 14-20, 24, 33-37, and 45 would be in condition for allowance if rewritten in independent form. These claims have been so amended and it is respectfully submitted that they are now in condition for allowance.

67. Applicants presented no other argument with respect to the patentability of claims 2-4, 8, 14-20, 24, 33-37, and 45.

68. On December 9, 1997, the Examiner entered a Notice of Allowability and Examiner's Amendment indicating claims 2-22, 24-28, and 33-41were allowable.

69. As shown in Appendix 4 of this opinion, the amendment amended claims 2, 11, 16, 20, 24, and 36 to correct grammatical and lack of antecedent basis errors.

70. In the Examiner's Amendment at pages 2-3, the examiner stated as follows:

> [T]he prior art of record fails to teach or fairly suggest an infrared imaging system or focal plane array having in combination with the other required elements, the means for correcting specified by independent claim 2, 24, 33 or 37.

71. Consistent with Office practice, the claims were re-numbered in the course of preparing the original application for issue, all as follows:

Chronological by original claim

Original claim number	Claim as re-numbered
1	Cancelled
2	1
3	2
4	5
5	6
6	7
7	8
8	9
9	12
10	13
11	14
12	19
13	20
14	3
15	4
16	10
17	11
18	21

Chronological by original claim

Original claim number	Claim as re-numbered
19	22
20	23
21	24
22	25
23	Cancelled
24	26
25	15
26	16
27	17
28	18
29	Cancelled
30	Cancelled
31	Cancelled
32	Cancelled
33	27
34	28
35	29
36	30
37	35
38	31
39	32
40	33
41	34
42	Cancelled
43	Cancelled
44	Cancelled
45	Cancelled
46	Cancelled
47	Cancelled
48	Cancelled
49	Cancelled
50	Cancelled

Chronological by original claim

Original claim number	Claim as re-numbered
51	Cancelled
52	Cancelled
53	Cancelled
54	Cancelled
55	Cancelled
56	Cancelled
57	Cancelled

Chronological by patent claim

Original claim number	Claim as re-numbered
2	1
3	2
14	3
15	4
4	5
5	6
6	7
7	8
8	9
16	10
17	11
9	12
10	13
11	14
25	15
26	16
27	17
28	18
12	19

Chronological by patent claim

Original claim number	Claim as re-numbered
13	20
18	21
19	22
20	23
21	24
22	25
24	26
33	27
34	28
35	29
36	30
38	31
39	32
40	33
41	34
37	35
1	Cancelled
23	Cancelled
29	Cancelled
30	Cancelled
31	Cancelled
32	Cancelled
42	Cancelled
43	Cancelled
44	Cancelled
45	Cancelled
46	Cancelled
47	Cancelled
48	Cancelled
49	Cancelled
50	Cancelled

Chronological by patent claim	
Original claim number	Claim as re-numbered
51	Cancelled
52	Cancelled
53	Cancelled
54	Cancelled
55	Cancelled
56	Cancelled
57	Cancelled

72. U.S. Patent 5,811,808 issued September 22, 1998, based on the original application and contained claims 1-35, all as shown in Appendix 5 of this opinion.

C. *Prosecution of reissue application*

73. Applicants filed reissue application 09/667,826 on September 21, 2000, seeking to reissue U.S. Patent 5,811,808.

74. Applicants presented amended versions of original patent claims 1-35 along with new reissue application claims 36-39 for consideration.

75. During prosecution the amended versions of original patent claims 1-35 were again amended to place them in their original form as found in the patent, reissue claims 36-39 were cancelled, and reissue claims 40-58 were added.

76. Ultimately, reissue claims 1, 5-7, 12-13, 15, 19, 21-22, 24-25, 40-50 and 52-58 were rejected, reissue claim 51 was objected to as a duplicate of claim 20, and claims 2-4, 8-11, 14, 16-18, 20, 23, and 26-35 were indicated as allowable.

77. Reissue application claims 1, 5-7, 12-13, 15, 19, 21-22, 24-25, 40-50 and 52-58 are before the Board in the appeal.

78. A copy of patent (reissue) claims 1, 5-7, 12-13, 15, 19, 21-22, 24-25 appears in Appendix 5 of this opinion. A copy of reissue application claims 40-50 and 52-58 appears in Appendix 6 of this opinion.

79. The Examiner has rejected reissue application claims 40-50 and 52-58 under 35 U.S.C. § 251 maintaining that the claims seek to "recapture" subject matter surrendered in obtaining allowance of the claims which appear in the patent sought to be reissued.

80. The Examiner based the rejection of claims 40-50 and 52-58 on the grounds that when faced in the original application with a rejection under 35 U.S.C. § 102 and 35 U.S.C. § 103 over the Lung and Masarik prior art patents, applicants made four significant amendments:

(1) First, applicants amended allowable dependent claim 2 to combine the limitations of allowable dependent claim 2 with rejected independent claim 1; original application claim 2 ultimately became patent claim 1.

(2) Second, applicants amended allowable dependent claim 24 to combine the limitations of allowable dependent claim 24 with rejected dependent claim 23 and rejected independent claim 1; original application claim 24 ultimately became patent claim 26.

(3) Third, applicants amended allowable dependent claim 33 to combine the limitations of allowable dependent claim 33 with rejected dependent claims 28-32 and rejected independent claim 29; original application claim 33 ultimately became patent claim 27.

(4) Fourth, applicants amended dependent claim 37 to combine limitations of allowable dependent claim 37 with rejected dependent claims 30 and

31, and rejected independent claim 29; original application claim 37 ultimately became patent claim 35.

D. *Examiner's Rejections*

(1)
35 U.S.C. § 251

81. The Examiner rejected reissue application claims 40-50 and 52-58 as being unpatentable under 35 U.S.C. § 251 for recapturing subject matter surrendered in obtaining allowance of claims during prosecution of the application which matured into the patent sought to be reissued.

82. The Examiner reasoned as follows (see Final Office Action entered January 17, 2002, pages 2-3):

> The reissue claims 40, 41, 42, 43, 52, and 58 delete a limitation ("parallel connected") from the patent claims. Therefore, the reissue claims are broader than the patent claims in the aspect of the electrical connection of the plurality of circuit elements. The broader aspect of the reissue claims relates to subject matter that applicant previously surrendered during the prosecution of the original application. The limitation ("parallel connected") omitted in the reissue claims was present in the claims of the original application (at least claims 2-4, 8, 24, 26, 37, 42, 44, and 45). The examiner's reasons for allowance in the original application stated that it was that limitation ("the means for correcting specified by independent claim 2, 24, 33 or 37" where the means for correcting specified a correction circuit including a plurality of parallel connected circuit elements and means for

> selectively electrically connecting said circuit elements into the detector readout circuit in response to stored offset correction values) which distinguished over a potential application of references Lung and Masarik et al. Applicant did not present on the record a counter statement or comment as to the examiner's reasons for allowance, and permitted the claims to issue. The omitted limitation is thus established as relating to subject matter previously surrendered.

83. The Examiner further reasoned as follows (see Final Office Action entered January 17, 2002, page 3):

> The reissue claim 53 deletes a limitation ("capacitors") from the patent claims. Therefore, the reissue claims are broader than the patent claims in the aspect of the electrical connection between the sample node and a reference voltage. The broader aspect of the reissue claims relates to subject matter that applicant previously surrendered during the prosecution of the original application. The limitation ("capacitors") omitted in the reissue claims was present in the claims of the original application (claim 32). The examiner's reasons for allowance in the original application stated that it was that limitation ("the means for correcting specified by independent claim 2, 24, 33 or 37" where the means for correcting specified a plurality of capacitors connected between said sample node and a reference voltage and a corresponding plurality of switches coupled in series with each respective capacitor and said reference voltage) which distinguished over a potential application of references Lung and Masarik et al. Applicant did not present on the record a counter statement or comment as to the examiner's reasons for allowance, and permitted the claims to issue. The omitted limitation is thus established as relating to subject matter previously surrendered.

84. The record supports the Examiner's findings with respect to what limitations do not appear in reissue application claims 40-50 and 52-58 which were present in claims 2, 24, 33, and 37 of the original application, as allowed.

(2)
35 U.S.C. § 112, First Paragraph

85. The Examiner rejected reissue application claims 40-50 and 52-58 as being unpatentable under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

86. The Examiner reasoned as follows (see Final Office Action entered January 17, 2002, page 4):

> The specification does not describe an infrared imaging system or an infrared focal plane array in which the circuit elements of the correction circuit in the means for separately correcting offsets in the detection signals are not parallel connected.

(3)
35 U.S.C. § 102

87. The Examiner rejected reissue application claims 1, 5, 21-22, 40, 42, and 48 as being unpatentable under 35 U.S.C. § 102(b) as being clearly anticipated by U.S. Patent 4,752,694, to Hegel, Jr. et al (Hegel).

88. The Examiner reasoned in-part as follows (see Final Office Action entered January 17, 2002, page 6):

> [Hegel discloses] means **60** for selectively electrically connecting the circuit elements **14** into the detector readout circuit in response to stored offset correction values.

(4)
35 U.S.C. § 103

89. The Examiner rejected reissue application claims 6, 7, 12, 13, 15, 19, 24, 25, 44-47, and 50 have also been rejected under 35 U.S.C. § 103(a) on the grounds that these claims are unpatentable over Hegel.

III. DISCUSSION – REJECTION UNDER 35 U.S.C. § 251

A. *The Prima Facie Case*

Our Findings of Fact 80-83 set out the basis upon which the Examiner made a recapture rejection. As noted in Finding 84, the record supports the Examiner's findings.

Basically, in the application which matured into the patent now sought to be reissued, the Examiner "objected to" originally filed dependent claim 2 (dependent on claim 1). Why? Because, it depended from claims that were rejected over the prior art. The Examiner indicated in the first Office action, however, that application claim 2 would be allowable if re-written in independent form.

Applicants proceeded to re-write application claim 2 by (1) canceling claim 1 and (2) combining limitations of allowable dependent claim 2 with rejected independent claim 1. Amended application claim 2 issued as patent claim 1.

Applicants also proceeded to re-write application claim 24 by (1) canceling claims 1 and 23, and (2) combining the limitations of allowable dependent claim 24 with rejected claims 1 and 23. Amended application claim 24 issued as patent claim 26.

Applicants also proceeded to re-write application claim 33 by (1) canceling claims 29-32, and (2) combining the limitations of allowable dependent claim 33 with rejected claims 29-32. Amended application claim 33 issued as patent claim 27.

Applicants further proceeded to re-write application claim 37 by (1) canceling claims 29-31, and (2) combining the limitations of allowable dependent claim 37 with rejected claims 29-31. Amended application claim 37 issued as patent claim 35.

The Examiner makes four points in Findings of Fact 82 and 83:

(1) the reissue claims 40, 41, 42, 43, 52, and 58 are broader than the patent claims with respect to the "parallel connected" limitation;

(2) the Examiner's reasons for allowance in the original application shows that the "parallel connected" limitation was surrendered;

(3) the reissue claim 53 is broader than the patent claims with respect to the "capacitors" limitation; and

(4) the "capacitors" limitation was surrendered as shown by the Examiner's reasons for allowance and because it was present in original application claim 32.

B. *Appellants' Response To The Examiner's Case*

Appellants argue at page 21 of the brief that "the present Examiner has mischaracterized the first Examiner's reason for allowance." We agree.

Contrary to the present Examiner's positions shown in Findings of Fact 82 and 83, the first Examiner's reason for allowance merely states as shown at Finding of Fact 70, that:

> [t]he prior art of record fails to teach or fairly suggest an infrared imaging system or focal plane array having in combination with the other required elements, the means for correcting specified by independent claim 2, 24, 33 or 37.

We find nothing in this statement that would lead an objective observer to conclude with respect to either "parallel connected" or "capacitors" that a deliberate surrender happened in order to avoid an obstacle to patentability. Yoon Ja Kim v. Conagra Foods, Inc., 465 F.3d 1312, 1323, 80 USPQ2d 1495, 1502 (Fed. Cir. 2006).

As to the Examiner's position that "capacitors" was surrendered because they were present in original claim 32, we find it highly relevant that claim 32 was rejected based on the prior art (Finding of Fact 56) and the limitations of allowable claim 33 were combined with rejected claims 29-32 to create patent claim 27. The Examiner sets forth no theory that supports surrender of an individual limitation in

a claim which was rejected based on prior art, nor does this Board know of such a theory.

The Examiner has shown that the reissue claims are broader than the patent claims, but has not shown that the broader aspects of the reissued claim relate to surrendered subject matter. Pannu v. Storz Instruments, Inc., 258 F.3d 1366, 1371, 59 USPQ2d 1597, 1600 (Fed. Cir. 2001).

IV. DISCUSSION – REJECTION UNDER 35 U.S.C. § 112

A. *The Prima Facie Case*

Our Findings of Fact 86 sets out the basis upon which the Examiner made a written description rejection.

The Examiner repeatedly states that the specification does not describe a system in which the "means for separately correcting offsets in the detection signals are not parallel connected" (Final Rejection at page 4, answer at page 5). However, Appellants' original specification contained claim 1 which did not include this limitation. This means that ultimately the Examiner's position is that given originally filed claim 1, an artisan could not build a "non-parallel" correcting means.

Thus, we see the Examiner's underlying position as an enablement issue where either an artisan would not know of any non-parallel equivalent, or the limitation "parallel connected" is essential to the claim. However, the Examiner does not explain why an artisan would not know of equivalents that are not parallel connected, and the Examiner does not explain why the "parallel connected" limitation is essential.

Therefore, we conclude the Examiner has not made a prima facie case with respect to the rejection under 35 U.S.C. § 112, first paragraph.

V. DISCUSSION – REJECTIONS UNDER 35 U.S.C. § § 102 AND 103

A. *The Prima Facie Case*

Our Findings of Fact 88 sets out the pivotal point upon which rests all the Examiner's prior art rejections. All the rejected claims require in some form a means for correcting comprising "means for selectively electrically connecting . . . in response to stored offset values" (reissue claim 1). It is the Examiner's position that this means for selectively connecting is described in Hegel at item 60 (Finding of Fact 88).

B. *Appellants' response to the Examiner's case*

Appellants argue at page 5 of the brief that the claimed "means for correcting offsets are distinctly different from Hegel's." We agree.

Appellants' claim limitation specifically requires that the selectively connecting is "in response to stored offset values." We find no such limitation described in Hegel. Rather, Hegel states that "switches [60 and 61] may be electronic switches controlled by a sequencer 62" (col. 2, lines 47-48). Thus, the selection is made by sequencer 62.

While we agree with the Examiner that Hegel reaches the same overall result as the claimed invention via offset correction values stored at means 70, we do not agree that output of means 70 performs the function of selectively connecting as required by the claim limitation. We find that at most the means 70 merely regulates the amount of the selectively connecting after the selective connection is made in response to sequencer 62.

Therefore, we conclude the Examiner has not made a prima facie case with respect to the rejections under 35 U.S.C. §§ 102 and 103.

VI. DECISION

Upon consideration of the record, and for the reasons given, the decision of the Examiner rejecting claims 40-50 and 52-58 under 35 U.S.C. § 251 based on recapture is reversed; the decision of the Examiner rejecting claims 40-50 and 52-58 under 35 U.S.C. § 112, first paragraph is reversed; the decision of the Examiner rejecting claims 1, 5, 21, 22, 40, 42, and 48 under 35 U.S.C. 102(b) is reversed; and the decision of the Examiner rejecting claims 6, 7, 12, 13, 15, 19, 24, 25, 44-47, and 50 under 35 U.S.C. § 103(a) is reversed.

REVERSED

rwk

Appendix 1

Drawings of application, as filed

Brief description of the drawings of Cannata et al., U.S. Patent 5,811,808, of which the present applicants seek reissue (drawing sheets 1-3, 7, and 9 are attached).

Figure 1 is a block schematic drawing of an infrared focal plane array imaging system in accordance with the present invention.

Figure 2 is a block schematic drawing of the focal plane array shown in Figure 1, in accordance with the present invention.

Figure 3A is a schematic drawing illustrating the readout cell circuitry associated with a single pixel of the focal plane array of Figure 2 in accordance with a preferred embodiment of the present invention employing current biasing of a microbolometer detector element.

Figure 3B is the readout circuit of Figure 3A further including an offset correction circuit in accordance with the present invention.

Figures 6A-6G are timing diagrams illustrating the timing signals employed in the readout circuit.

Figure 7 is a graphical representation of an example of offset correction provided for several pixels of the focal plane array in accordance with the present invention.

Figure 10 is an alternate embodiment of the offset correction circuit illustrated in Figure 3 employing a network of fixed current sources.

Figure 11 is a schematic drawing of another alternate embodiment of the offset correction circuit of Figure 3 employing a network of fixed current sources switchably connected between the voltage source and the microbolometer detector element.

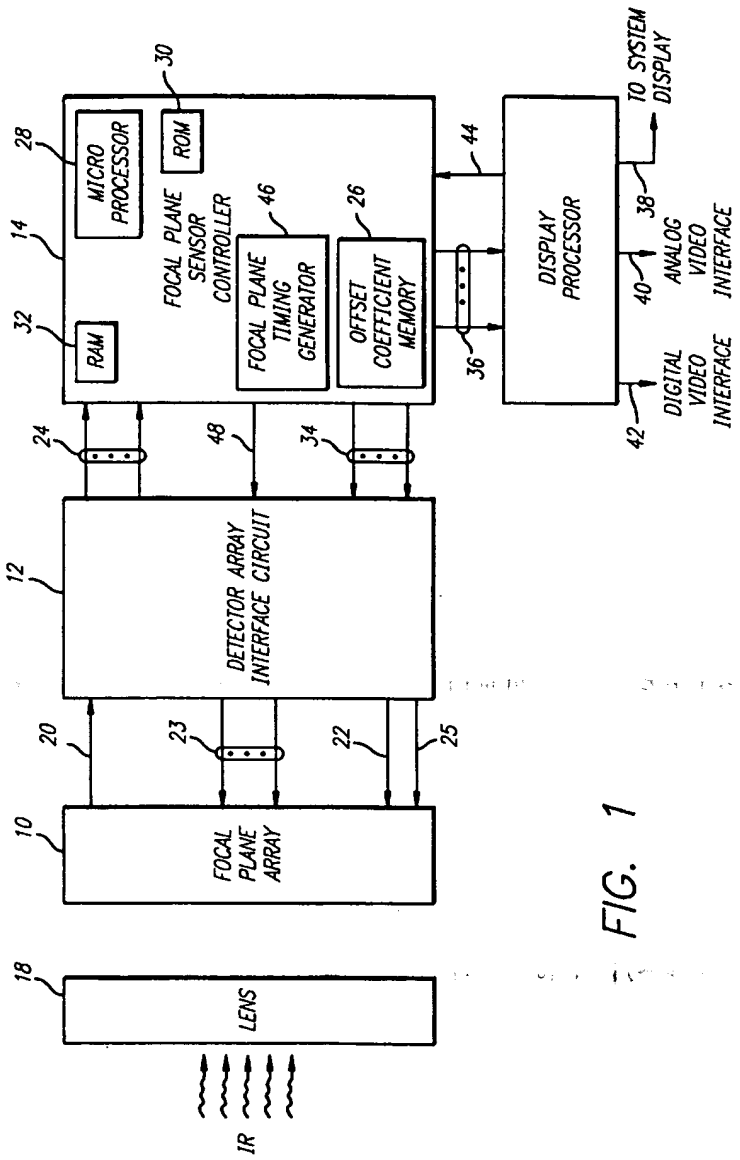

30
28
MICRO PROCESSOR
ROM
14
FOCAL PLANE SENSOR CONTROLLER
46
FOCAL PLANE TIMING GENERATOR
26
OFFSET COEFFICIENT MEMORY
32
RAM
44
DISPLAY PROCESSOR
TO SYSTEM DISPLAY
38
40
ANALOG VIDEO INTERFACE
36
42
DIGITAL VIDEO INTERFACE
24
48
34
12
DETECTOR ARRAY INTERFACE CIRCUIT
20
23
22
25
10
FOCAL PLANE ARRAY
18
LENS
IR

FIG. 1

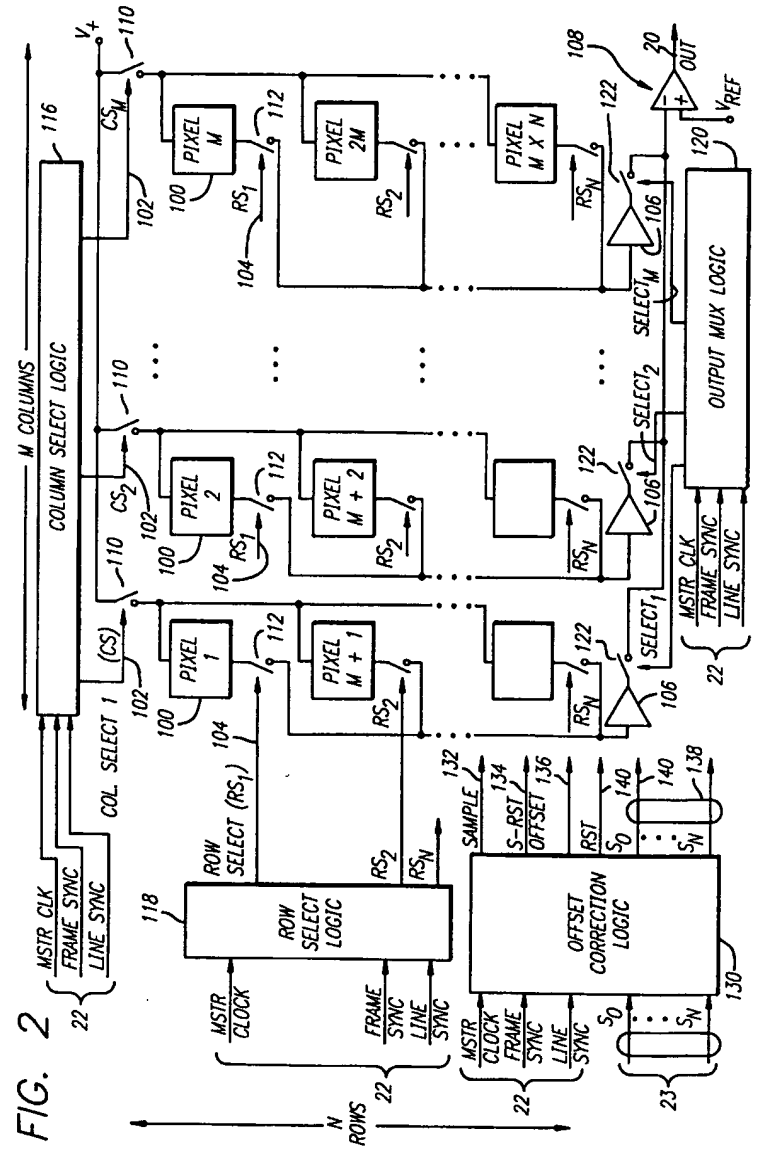
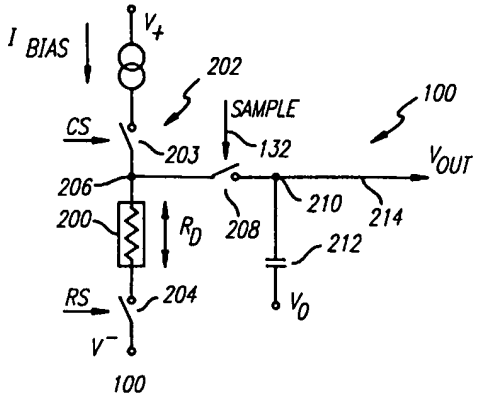

M COLUMNS
COLUMN SELECT LOGIC
116
V_+
110
CS_M
CS_2
(CS)
102
COL SELECT 1
PIXEL M
PIXEL 2M
PIXEL M X N
PIXEL 2
PIXEL M + 2
PIXEL 1
PIXEL M + 1
100
112
RS_1
RS_2
RS_N
104
122
106
$SELECT_M$
$SELECT_2$
$SELECT_1$
108
20
OUT
V_{REF}
120
OUTPUT MUX LOGIC
MSTR CLK
FRAME SYNC
LINE SYNC
22
ROW SELECT (RS_1)
ROW SELECT LOGIC
118
MSTR CLOCK
FRAME SYNC
LINE SYNC
N ROWS
SAMPLE
132
S-RST
134
OFFSET
136
RST
140
S_0
S_N
138
OFFSET CORRECTION LOGIC
130
23

FIG. 2

FIG. 3A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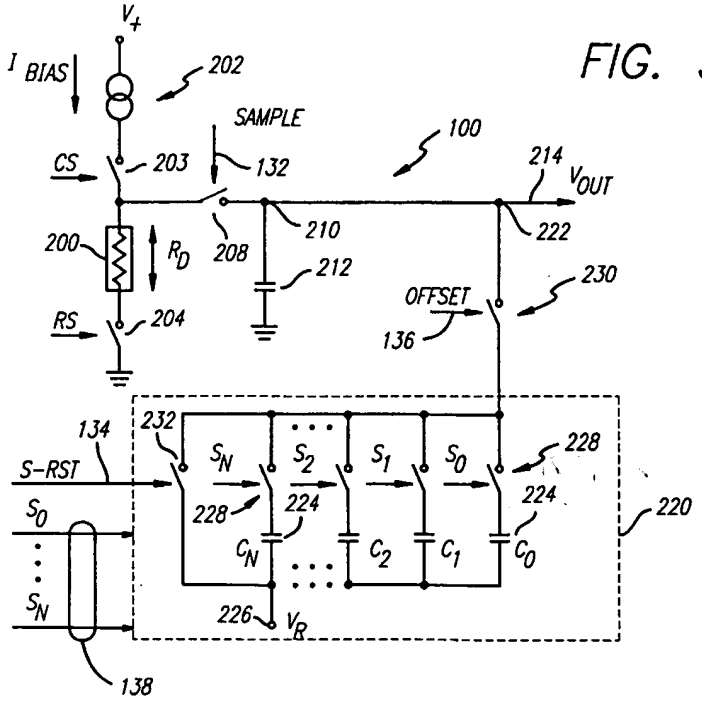
V+
202
SAMPLE
100
CS
203
132
VOUT
206
210
214
200
RD
208
212
RS
204
VO
V−
100

FIG. 3B


V+
I BIAS
202
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100
214
VOUT
CS
203
132
210
222
200
RD
208
212
230
OFFSET
RS
204
136
134
232
228
220
S-RST
SN
S2
S1
S0
224
C0
C1
C2
CN
226
VR
138

FIG. 6A

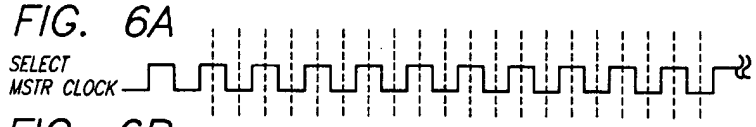


FIG. 6B

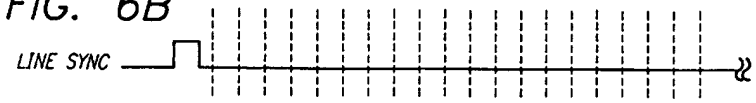


FIG. 6C

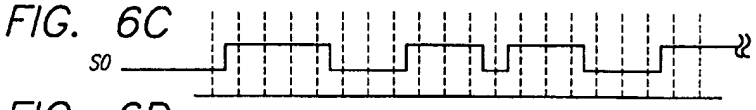


FIG. 6D

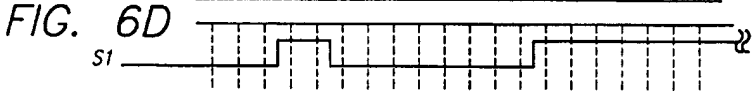


FIG. 6E

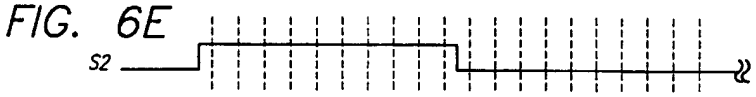


FIG. 6F

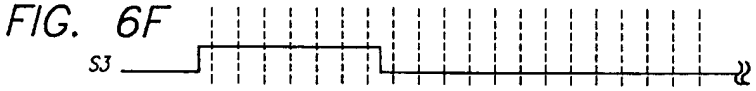


FIG. 6G

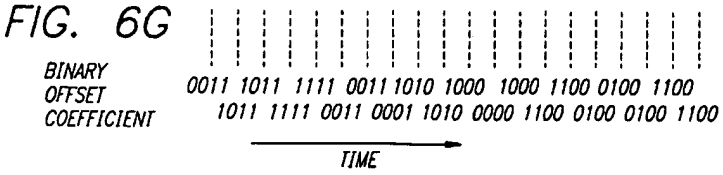


FIG. 7

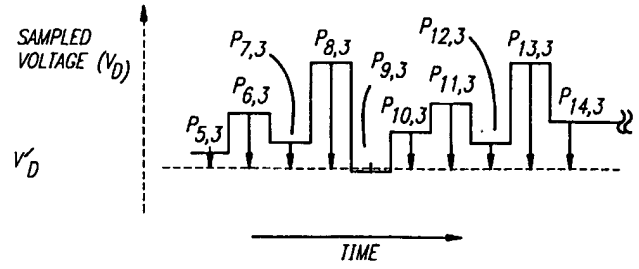
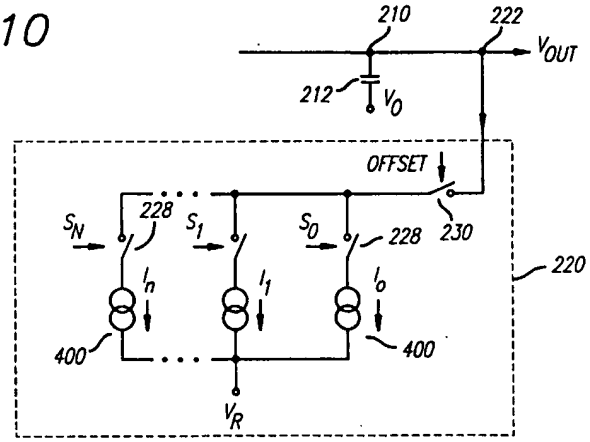


FIG. 10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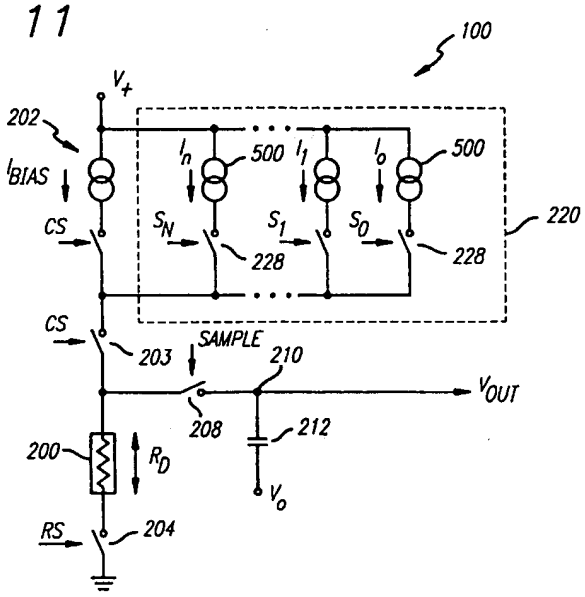
222
V_{OUT}
212
V_0
OFFSET
S_N
228
S_1
S_0
228
230
220
I_n
I_1
I_0
400
400
V_R

FIG. 11


100
V_+
202
I_{BIAS}
I_n
500
I_1
I_0
500
220
CS
S_N
S_1
S_0
228
228
CS
203
SAMPLE
210
V_{OUT}
208
212
200
R_D
V_o
RS
204

Appendix 2

Claims Of Original Patent Application 08/429,317, As Filed

1. An infrared imaging system, comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising

means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and

means for separately correcting offsets in the detection signals provided from the plurality of elements in the detector array to compensate for nonuniformities in the detector elements; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

2. An infrared imaging system as set out in claim 1, wherein said means for correcting comprises:

a correction circuit including a plurality of parallel connected circuit elements; and

means for selectively electrically connecting said circuit elements into the detector readout circuit in response to said stored offset correction values.

3. An infrared imaging system as set out in claim 2, wherein said plurality of parallel connected circuit elements comprise a plurality of capacitors.

4. An infrared imaging system as set out in claim 2, wherein said means for selectively connecting comprises a plurality of switches, equal in number to said plurality of parallel connected circuit elements and connected in series therewith.

5. An infrared imaging system as set out in claim 1, wherein said offset correction values are binary values separately and wherein said means for storing comprises a digital memory.

6. An infrared imaging system as set out in claim 5, wherein said digital memory stores a separate binary offset correction value for each detector element in the array.

7. An infrared imaging system as set out in claim 2, wherein said plurality of detector elements are arranged in a plurality of rows and columns and wherein said means for correcting comprises a separate offset correction circuit for each column and wherein said means for providing said offset correction values provides said offset correction values in a time multiplexed manner to said means for correcting.

8. An infrared imaging system as set out in claim 2, wherein said plurality of parallel connected circuit elements comprise a plurality of constant current sources.

9. An infrared imaging system as set out in claim 2, wherein said array of detector elements and said readout circuit are formed as a single monolithic integrated circuit chip.

10. An infrared imaging system as set out in claim 2, wherein said plurality of detector elements comprise microbolometer detector elements.

11. An infrared imaging system as set out in claim 10, wherein means for biasing comprises a constant current source coupled to said microbolometer detector elements.

12. An infrared imaging system as set out in claim 2, wherein said output means comprises one or more output buffers.

13. An infrared imaging system as set out in claim 2, wherein said focal plane array further comprises a differential amplifier with first and second inputs wherein the first input is electrically connected to the readout circuit so as to receive the detection signals and wherein the second input is connected to an adjustable reference voltage.

14. An infrared imaging system as set out in claim 3, wherein said capacitors

have capacitances of $2^N C_0$, respectively, where C_0 is a fixed capacitance and N is a nonnegative integer.

15. An infrared imaging system as set out in claim 14, wherein there are four capacitors having respective capacitances of C_0, $2C_0$, $4C_0$ and $8C_0$.

16. An infrared imaging system as set out in claim 8, wherein said current sources provide substantially constant currents of $2^N I_0$, respectively, when coupled into said readout circuit by said means for connecting, where I_0 is a fixed current value and N is a nonnegative integer.

17. An infrared imaging system as set out in claim 16, wherein there are four constant current sources providing substantially constant currents of I_0, $2I_0$, $4I_0$ and $8I_0$.

18. An infrared imaging system as set out in claim 2, further comprising timing means for providing focal plane timing signals to said readout circuit.

19. An infrared imaging system as set out in claim 18, wherein said readout circuit further comprises offset correction logic means for controlling the means for correcting in response to said timing signals provided from the timing means.

20. An infrared imaging system as set out in claim 19, wherein said offset correction logic means receives said offset correction values from said means for storing and provide them to said means for correcting in response to said timing signals.

21. An infrared imaging system as set out in claim 2, further comprising means, coupled to said output means, for analog to digital converting the corrected detection signals and providing corresponding image data for each detector element.

22. An infrared imaging system as set out in claim 21, further comprising a memory for temporarily storing image data corresponding to all the detector elements of the array.

23. An infrared imaging system as set out in claim 1, wherein said readout circuit comprises a plurality of readout cells in number to the plurality of detector elements and wherein said means for correcting comprises an offset correction circuit in each readout cell of the readout circuit.

24. An infrared imaging system as set out in claim 23, wherein each offset

correction circuit comprises a plurality of parallel connected circuit elements and means for selectively electrically connecting said circuit elements into the readout cell in response to the stored offset correction value corresponding to said readout cell.

25. An infrared imaging system as set out in claim 10, wherein said means for biasing comprises a fixed voltage source coupled to said microbolometers.

26. An infrared imaging system as set out in claim 25, wherein said means for correcting comprises a plurality of substantially constant current sources selectively coupled to said voltage source and in parallel with said microbolometer.

27. An infrared imaging system as set out in claim 26, wherein said means for correcting further comprises a plurality of switches coupled in series with respective constant current sources.

28. An infrared imaging system as set out in claim 27, wherein said offset correction values comprise an on or off signal supplied to each of said switches.

29. An infrared focal plane array, comprising:

a plurality of detector elements configured in a two dimensional array; and

a readout circuit electrically coupled to said plurality of detector elements and structurally integrated therewith, said readout circuit comprising:

means for biasing the detector elements so as to provide an analog detection signal from each detector element corresponding to the infrared radiation incident thereon; and

means for correcting the analog detection signal from each detector element by a discrete offset correction and providing a corrected analog detection signal, the discrete offset correction varying from detector element to detector element.

30. A focal plane array as set out in claim 29, wherein said analog detection signal is a voltage signal and the discrete offset correction comprises an offset correction voltage added to, or subtracted from, the voltage signal.

31. A focal plane array as set out in claim 30, wherein said readout circuit includes a sample and hold capacitor and wherein the detection voltage signal is provided at a sample node coupled to the sample and hold capacitor and wherein said means for correcting subtracts or adds a variable amount of charge from said sample and hold capacitor to provide a corrected voltage signal at said sample node.

32. A focal plane array as set out in claim 31, wherein said means for correcting comprises a plurality of capacitors connected between said sample node and a reference voltage and a corresponding plurality of switches coupled in series with each respective capacitor and said reference voltage.

33. A focal plane array as set out in claim 32, wherein said plurality of switches are selectively turned on or off to provide a desired amount of discrete offset correction for each detector element.

34. An infrared focal plane array as set out in claim 33, wherein said readout circuit further comprises means for controlling said means for correcting so as to selectively open and close said plurality of switches in a time multiplexed manner during readout of a plurality of separate detector elements.

35. An infrared focal plane array as set out in claim 33, wherein said detector elements comprise microbolometer detector elements.

36. An infrared focal plane array as set out in claim 35, wherein said means for said biasing comprises a constant current source coupled to said microbolometer elements and said sample and hold capacitor.

37. An infrared focal plane array as set out in claim 31, wherein said means for correcting comprises a plurality of parallel connected constant current sources connected between said sample node and reference voltage and a plurality of switches corresponding to said plurality of constant current sources and respectively coupled in series therewith.

38. An infrared focal plane array as set out in claim 31, wherein said readout circuit further comprises a differential amplifier having first and second inputs, the first input thereof coupled to said sample node and said second input thereof coupled to a adjustable voltage source.

39. An infrared focal plane array as set out in claim 38, wherein said readout circuit further comprises a feedback capacitor coupled between the output of the differential amplifier and said first input thereof.

40. An infrared focal plane array as set out in claim 39, wherein said readout circuit further comprises a switch coupled between and parallel with said feedback capacitor between the output of the differential amplifier and the first input thereof.

41. An infrared focal plane array as set out in claim 29 wherein said plurality of detector elements and said readout circuit are formed as a single monolithic integrated circuit wherein said readout circuit acts as a substrate for said detector elements.

42. through 57. (Not reproduced)

Appendix 3

September 9, 1997 All Claims As Amended In Response To Non-Final Action In Original Patent Application

(matter underlined added by the amendment)
(matter in [brackets] deleted by the amendment)

1. (Cancelled)

2. An infrared imaging system [as set out in claim 1], comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising

means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and

means for separately correcting offsets in the detection signals provided from the plurality of elements in the detector array to compensate for nonuniformities in the detector elements, wherein said means for correcting comprises:

a correction circuit including a plurality of parallel connected circuit elements; and

means for selectively electrically connecting said circuit elements into the detector readout circuit in response to said stored offset correction values; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

3. (NO CHANGE)

4. (NO CHANGE)

5. An infrared imaging system as set out in claim [1] 2, wherein said offset correction values are binary values separately and wherein said means for storing comprises a digital memory.

6. (NO CHANGE)

7. An infrared imaging system as set out in claim [1] 2, wherein said plurality of detector elements are arranged in a plurality of rows and columns and wherein said means for correcting comprises a separate offset correction circuit for each column and wherein said means for providing said offset correction values provides said offset correction values in a time multiplexed manner to said means for correcting.

8. (NO CHANGE)

9. An infrared imaging system as set out in claim [1] 2, wherein said array of detector elements and said readout circuit are formed as a single monolithic integrated circuit chip.

10. An infrared imaging system as set out in claim [1] 2, wherein said plurality of detector elements comprise microbolometer detector elements.

11. (NO CHANGE)

12. An infrared imaging system as set out in claim [1] 2, wherein said output means comprises one or more output buffers.

13. An infrared imaging system as set out in claim [1] 2, wherein said focal plane array further comprises a differential amplifier with first and second inputs wherein the first input is electrically connected to the readout circuit so as to receive the detection signals and wherein the second input is connected to an adjustable reference voltage.

14. through 20. (NO CHANGE)

21. An infrared imaging system as set out in claim [1] 2, further comprising means, coupled to said output means, for analog to digital converting the corrected detection signals and providing corresponding image data for each detector element.

22. (NO CHANGE)

23. (CANCELLED)

24. An infrared imaging system [as set out in claim 23], comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising a plurality of readout cells equal in number to the plurality of detector elements, means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and means for separately correcting offsets in the detection signals provided from the plurality of elements in the detector array to compensate for nonuniformities in the detector elements, wherein said means for correcting comprises an offset correction circuit in each readout cell of the readout circuit and wherein each offset correction circuit comprises a plurality of parallel connected circuit elements and means for selectively electrically connecting said circuit elements into the readout cell in response to a stored offset correction value corresponding to said readout cell; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

25. An infrared imaging system as set out in claim 10, wherein said means for biasing comprises a fixed voltage source coupled to said [microbolometers] microbolometer detector elements.

26. An infrared imaging system as set out in claim 25, wherein said means for correcting comprises a plurality of substantially constant current sources selectively coupled to said voltage source and in parallel with said microbolometer detector elements.

27. through 28. (NO CHANGE)

29. through 32. (CANCELLED)

33. An infrared focal plane array [as set out in claim 32], comprising:

a plurality of detector elements configured in a two dimensional array; and

a readout circuit electrically coupled to said plurality of detector elements and structurally integrated therewith, said readout circuit comprising:

a sample and hold capacitor;

means for biasing the detector elements so as to provide an analog detection signal from each detector element corresponding to the infrared radiation incident thereon, wherein the analog detection signal is a voltage signal provided at a sample node coupled to the sample and hold capacitor; and

means for correcting the analog detection signal from each detector element by a discrete offset correction and providing a corrected analog detection signal, wherein the discrete offset correction varies from detector element to detector element and comprises an offset correction voltage added to, or subtracted from, the analog detection signal, wherein said means for correcting subtracts or adds a variable amount of charge from said sample and hold capacitor to provide a corrected voltage signal at said sample node, and wherein said means for correcting comprises a plurality of capacitors connected between said sample node and a reference voltage and a corresponding plurality of switches coupled in series with each respective capacitor and said reference voltage, wherein said plurality of switches are selectively turned on or off to provide a desired amount of discrete offset correction for each detector element.

34. through 36. (NO CHANGE)

37. An infrared focal plane array [as set out in claim 31], comprising:

a plurality of detector elements configured in a two dimensional array; and

a readout circuit electrically coupled to said plurality of detector elements and structurally integrated therewith, said readout circuit comprising:

a sample and hold capacitor;

means for biasing the detector elements so as to provide an analog detection signal from each detector element corresponding to the infrared radiation incident thereon, wherein the analog detection signal is a voltage signal provided at a sample node coupled to the sample and hold capacitor; and

means for correcting the analog detection signal from each detector element by a discrete offset correction and providing a corrected analog detection signal, wherein the discrete offset correction varies from detector element to detector element and comprises an offset correction voltage added to, or subtracted from, the voltage signal, wherein said means for correcting subtracts or adds a variable amount of charge from said sample and hold capacitor to provide a corrected voltage signal at said sample node, and wherein said means for correcting comprises a plurality of parallel connected constant current sources connected between said sample node and reference voltage and a plurality of switches corresponding to said plurality of constant current sources and respectively coupled in series therewith.

38. An infrared focal plane array as set out in claim [31] 33, wherein said readout circuit further comprises a differential amplifier having first and second inputs, the first input thereof coupled to said sample node and said second input thereof coupled to a adjustable voltage source.

39. through 40. (NO CHANGE)

41. An infrared focal plane array as set out in claim [29] 33 wherein said plurality of detector elements and said readout circuit are formed as a single monolithic integrated circuit wherein said readout circuit acts as a substrate for said detector elements.

42. through 57. (CANCELLED)

Appendix 4

December 9, 1997 Claims 2, 11, 16, 20, 24, 36, and 37, As Amended at Allowance

(matter underlined added by the amendment)
(matter in [brackets] deleted by the amendment)

2. An infrared imaging system, comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising

means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and

means for separately correcting offsets in the detection signals provided from the plurality of elements in the detector array to compensate for nonuniformities in the detector elements, wherein said means for correcting comprises:

a correction circuit including a plurality of parallel connected circuit elements; and

means for selectively electrically connecting said circuit elements into the detector readout circuit in response to [said] stored offset correction values; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

11. An infrared imaging system as set out in claim 10, wherein said means for biasing comprises a constant current source coupled to said microbolometer detector elements.

16. An infrared imaging system as set out in claim 8, wherein said current sources provide substantially constant currents of $2^N I_0$, respectively, when coupled into said readout circuit by said means for selectively connecting, where I_0 is a fixed current value and N is a nonnegative integer.

20. An infrared imaging system as set out in claim 19, wherein said offset correction logic means receives said offset correction values from said means for storing and [provide] provides them to said means for correcting in response to said timing signals.

24. An infrared imaging system, comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising a plurality of readout cells equal in number to the plurality of detector elements, means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and means for separately correcting offsets in the detection signals provided from the plurality of elements in the detector array to compensate for nonuniformities in the detector elements, wherein said means for correcting comprises an offset correction circuit in each readout cell of the readout circuit and wherein each offset correction circuit comprises a plurality of parallel connected circuit elements and means for selectively electrically connecting said circuit elements into the readout cell in response to [a] the stored offset correction value corresponding to said readout cell; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

36. An infrared focal plane array as set out in claim 35, wherein said means for said biasing comprises a constant current source coupled to said microbolometer detector elements and said sample and hold capacitor.

37. An infrared focal plane array, comprising:

a plurality of detector elements configured in a two dimensional array; and

a readout circuit electrically coupled to said plurality of detector elements and structurally integrated therewith, said readout circuit comprising:

a sample and hold capacitor;

means for biasing the detector elements so as to provide an analog detection signal from each detector element corresponding to the infrared radiation incident thereon, wherein the analog detection signal is a voltage signal provided at a sample node coupled to the sample and hold capacitor; and

means for correcting the analog detection signal from each detector element by a discrete offset correction and providing a corrected analog detection signal, wherein the discrete offset correction varies from detector element to detector element and comprises an offset correction voltage added to, or subtracted from, the voltage signal, wherein said means for correcting subtracts or adds a variable amount of charge from said sample and hold capacitor to provide a corrected voltage signal at said sample node, and wherein said means for correcting comprises a plurality of parallel connected constant current sources connected between said sample node and a reference voltage and a plurality of switches corresponding to said plurality of constant current sources and respectively coupled in series therewith.

Appendix 5

CLAIMS OF U.S. PATENT 5,811,808, AS RENUMBERED AT ALLOWANCE

1. An infrared imaging system, comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising

means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and

means for separately correcting offsets in the detection signals provided from the plurality of elements in the detector array to compensate for nonuniformities in the detector elements, wherein said means for correcting comprises:

a correction circuit including a plurality of parallel connected circuit elements; and

means for selectively electrically connecting said circuit elements into the detector readout circuit in response to stored offset correction values; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

2. An infrared imaging system as set out in claim 1, wherein said plurality of parallel connected circuit elements comprise a plurality of capacitors.

3. An infrared imaging system as set out in claim 2, wherein said capacitors have capacitances of $2^N C_0$, respectively, where C_0 is a fixed capacitance and N is a nonnegative integer.

4. An infrared imaging system as set out in claim 3, wherein there are four capacitors having respective capacitances of C_0, $2C_0$, $4C_0$ and $8C_0$.

5. An infrared imaging system as set out in claim 1, wherein said means for selectively connecting comprises a plurality of switches, equal in number to said plurality of parallel connected circuit elements and connected in series therewith.

6. An infrared imaging system as set out in claim 1, wherein said offset correction values are binary values and wherein said means for storing comprises a digital memory.

7. An infrared imaging system as set out in claim 6, wherein said digital memory stores a separate binary offset correction value for each detector element in the array.

8. An infrared imaging system as set out in claim 1, wherein said plurality of detector elements are arranged in a plurality of rows and columns and wherein said means for correcting comprises a separate offset correction circuit for each column and wherein said means for providing said offset correction values provides said offset correction values in a time multiplexed manner to said means for correcting.

9. An infrared imaging system as set out in claim 1, wherein said plurality of parallel connected circuit elements comprise a plurality of constant current sources.

10. An infrared imaging system as set out in claim 9, wherein said current sources provide substantially constant currents of $2^N I_0$, respectively, when coupled into said readout circuit by said means for selectively connecting, where I_0 is a fixed current value and N is a nonnegative integer.

11. An infrared imaging system as set out in claim 10, wherein there are four constant current sources providing substantially constant currents of I_0, $2I_0$, $4I_0$ and $8I_0$.

12. An infrared imaging system as set out in claim 1, wherein said array of detector elements and said readout circuit are formed as a single monolithic integrated circuit chip.

13. An infrared imaging system as set out in claim 1, wherein said plurality

of detector elements comprise microbolometer detector elements.

14. An infrared imaging system as set out in claim 13, wherein said means for biasing comprises a constant current source coupled to said microbolometer detector elements.

15. An infrared imaging system as set out in claim 13, wherein said means for biasing comprises a fixed voltage source coupled to said microbolometer detector elements.

16. An infrared imaging system as set out in claim 15, wherein said means for correcting comprises a plurality of substantially constant current sources selectively coupled to said voltage source and in parallel with said microbolometer detector elements.

17. An infrared imaging system as set out in claim 16, wherein said means for correcting further comprises a plurality of switches coupled in series with respective constant current sources.

18. An infrared imaging system as set out in claim 17, wherein said offset correction values comprise an on or off signal supplied to each of said switches.

19. An infrared imaging system as set out in claim 1, wherein said output means comprises one or more output buffers.

20. An infrared imaging system as set out in claim 1, wherein said focal plane array further comprises a differential amplifier with first and second inputs wherein the first input is electrically connected to the readout circuit so as to receive the detection signals and wherein the second input is connected to an adjustable reference voltage.

21. An infrared imaging system as set out in claim 1, further comprising timing means for providing focal plane timing signals to said readout circuit.

22. An infrared imaging system as set out in claim 21, wherein said readout circuit further comprises offset correction logic means for controlling the means for correcting in response to said timing signals provided from the timing means.

23. An infrared imaging system as set out in claim 22, wherein said offset correction logic means receives said offset correction values from said means for storing and provide them to said means for correcting in response to said timing signals.

24. An infrared imaging system as set out in claim 1, further comprising means, coupled to said output means, for analog to digital converting the corrected detection signals and providing corresponding image data for each detector element.

25. An infrared imaging system as set out in claim 24, further comprising a memory for temporarily storing image data corresponding to all the detector elements of the array.

26. An infrared imaging system, comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising a plurality of readout cells equal in number to the plurality of detector elements, means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and means for separately correcting offsets in the detection signals provided from the plurality of elements in the detector array to compensate for nonuniformities in the detector elements, wherein said means for correcting comprises an offset correction circuit in each readout cell of the readout circuit and wherein each offset correction circuit comprises a plurality of parallel connected circuit elements and means for selectively electrically connecting said circuit elements into the readout cell in response to a stored offset correction value corresponding to said readout cell; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

27. An infrared focal plane array, comprising:

a plurality of detector elements configured in a two dimensional array; and

a readout circuit electrically coupled to said plurality of detector elements

and structurally integrated therewith, said readout circuit comprising:

a sample and hold capacitor;

means for biasing the detector elements so as to provide an analog detection signal from each detector element corresponding to the infrared radiation incident thereon, wherein the analog detection signal is a voltage signal provided at a sample node coupled to the sample and hold capacitor; and

means for correcting the analog detection signal from each detector element by a discrete offset correction and providing a corrected analog detection signal, wherein the discrete offset correction varies from detector element to detector element and comprises an offset correction voltage added to, or subtracted from, the analog detection signal, wherein said means for correcting subtracts or adds a variable amount of charge from said sample and hold capacitor to provide a corrected voltage signal at said sample node, and wherein said means for correcting comprises a plurality of capacitors connected between said sample node and a reference voltage and a corresponding plurality of switches coupled in series with each respective capacitor and said reference voltage, wherein said plurality of switches are selectively turned on or off to provide a desired amount of discrete offset correction for each detector element.

28. An infrared focal plane array as set out in claim 27, wherein said readout circuit further comprises means for controlling said means for correcting so as to selectively open and close said plurality of switches in a time multiplexed manner during readout of a plurality of separate detector elements.

29. An infrared focal plane array as set out in claim 27, wherein said detector elements comprise microbolometer detector elements.

30. An infrared focal plane array as set out in claim 29, wherein said means for said biasing comprises a constant current source coupled to said microbolometer detector elements and said sample and hold capacitor.

31. An infrared focal plane array as set out in claim 27, wherein said readout circuit further comprises a differential amplifier having first and second inputs, the first input thereof coupled to said sample node and said second input thereof coupled to a adjustable voltage source.

32. An infrared focal plane array as set out in claim 31, wherein said readout

circuit further comprises a feedback capacitor coupled between the output of the differential amplifier and said first input thereof.

33. An infrared focal plane array as set out in claim 32, wherein said readout circuit further comprises a switch coupled between and parallel with said feedback capacitor between the output of the differential amplifier and the first input thereof.

34. An infrared focal plane array as set out in claim 27 wherein said plurality of detector elements and said readout circuit are formed as a single monolithic integrated circuit wherein said readout circuit acts as a substrate for said detector elements.

35. An infrared focal plane array, comprising:

a plurality of detector elements configured in a two dimensional array; and

a readout circuit electrically coupled to said plurality of detector elements and structurally integrated therewith, said readout circuit comprising:

a sample and hold capacitor;

means for biasing the detector elements so as to provide an analog detection signal from each detector element corresponding to the infrared radiation incident thereon, wherein the analog detection signal is a voltage signal provided at a sample node coupled to the sample and hold capacitor; and

means for correcting the analog detection signal from each detector element by a discrete offset correction and providing a corrected analog detection signal, wherein the discrete offset correction varies from detector element to detector element and comprises an offset correction voltage added to, or subtracted from, the voltage signal, wherein said means for correcting subtracts or adds a variable amount of charge from said sample and hold capacitor to provide a corrected voltage signal at said sample node, and wherein said means for correcting comprises a plurality of parallel connected constant current sources connected between said sample node and a reference voltage and a plurality of switches corresponding to said plurality of constant current sources and respectively coupled in series therewith.

Appendix 6

The Reissue Claims On Appeal

Claims 1, 5-7, 12, 13, 15, 19, 21, 22, 24, and 25. (Unchanged from patent).

40. An infrared imaging system, comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and means for separately correcting offsets in the detection signals provided from the plurality of elements in the detector array to compensate for nonuniformities in the detector elements, wherein said means for correcting comprises:

a correction circuit including a plurality of circuit elements; and

means for selectively electrically connecting said circuit elements into the detector readout circuit in response to stored offset correction values; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

41. An infrared imaging system as set out in claim 40, wherein said plurality of circuit elements comprise a plurality of capacitors.

42. An infrared imaging system as set out in claim 40, wherein said means for selectively connecting comprises a plurality of switches, equal in number to said plurality of circuit elements and connected in series therewith.

43. An infrared imaging system as set out in claim 40, wherein said plurality of circuit elements comprise a plurality of constant current sources.

44. An infrared imaging system as set out in claim 40, further comprising means, coupled to said output means, for analog to digital converting the corrected detection signals and providing corresponding image data for each detector element.

45 An infrared imaging system as set out in claim 40, wherein said plurality of detector elements comprise microbolometer detector elements.

46. An infrared imaging system as set out in claim 40, wherein said offset correction values are binary values and wherein said means for storing comprises a digital memory.

47. An infrared imaging system as set out in claim 40, wherein said array of detector elements and said readout circuit are formed as a single monolithic integrated circuit chip.

48. An infrared imaging system as set out in claim 40, further comprising timing means for providing focal plane timing signals to said readout circuit.

49 An infrared imaging system as set out in claim 40, wherein said plurality of detector elements are arranged in a plurality of rows and columns and wherein said means for correcting comprises a separate offset correction circuit for each column and wherein said means for providing said offset correction values provides said offset correction values in a time multiplexed manner to said means for correcting.

50. An infrared imaging system as set out in claim 40, wherein said output means comprises one or more output buffers.

51. (Not on Appeal)

52. An infrared imaging system, comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising a plurality of readout cells equal in number to the plurality of detector elements, means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and means for separately correcting offsets in the detection signals provided from the plurality of elements in the detector array to compensate for nonuniformities in the detector elements, wherein said means for correcting comprises an offset correction circuit in each readout cell of the readout circuit and wherein each offset correction circuit comprises a plurality of circuit elements and means for selectively electrically connecting said circuit elements into the readout cell in response to a stored offset correction value corresponding to said readout cell; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

53. An infrared focal plane array, comprising:

a plurality of detector elements configured in a two dimensional array; and

a readout circuit electrically coupled to said plurality of detector elements and structurally integrated therewith, said readout circuit comprising:

a sample and hold capacitor;

means for biasing the detector elements so as to provide an analog detection signal from each detector element corresponding to the infrared radiation incident thereon, wherein the analog detection signal is a voltage signal provided at a sample node coupled to the sample and hold capacitor; and

means for correcting the analog detection signal from each detector element by a discrete offset correction and providing a corrected analog detection signal, wherein the discrete offset correction varies from detector element to detector element and comprises an offset correction voltage added to, or subtracted from, the analog detection signal, wherein said means for correcting subtracts or adds a variable amount of charge from said sample and hold capacitor to provide a corrected voltage signal at said sample node, and wherein said means for correcting comprises a plurality of circuit elements connected between said sample node and a reference voltage and a corresponding plurality of switches coupled in series with each respective circuit element and said reference voltage, wherein said plurality of switches selectively provide a desired amount of discrete offset correction for each detector element.

54. An infrared focal plane array as set out in claim 53, wherein said readout circuit further comprises means for controlling said means for correcting so as to selectively open and close said plurality of switches in a time multiplexed manner during readout of a plurality of separate detector elements.

55. An infrared focal plane array as set out in claim 53, wherein said detector elements comprise microbolometer detector elements.

56. An infrared focal plane array as set out in claim 53, wherein said readout circuit further comprises a differential amplifier having first and second inputs, the

first input thereof coupled to said sample node and said second input thereof coupled to a adjustable voltage source.

57. An infrared focal plane array as set out in claim 53 wherein said plurality of detector elements and said readout circuit are formed as a single monolithic integrated circuit wherein said readout circuit acts as a substrate for said detector elements.

58. An infrared focal plane array, comprising:

a plurality of detector elements configured in a two dimensional array; and

a readout circuit electrically coupled to said plurality of detector elements and structurally integrated therewith, said readout circuit comprising:

a sample and hold capacitor;

means for biasing the detector elements so as to provide an analog detection signal from each detector element corresponding to the infrared radiation incident thereon, wherein the analog detection signal is a voltage signal provided at a sample node coupled to the sample and hold capacitor; and

means for correcting the analog detection signal from each detector element by a discrete offset correction and providing a corrected analog detection signal, wherein the discrete offset correction varies from detector element to detector element and comprises an offset correction voltage added to, or subtracted from, the voltage signal, wherein said means for correcting subtracts or adds a variable amount of charge from said sample and hold capacitor to provide a corrected voltage signal at said sample node, and wherein said means for correcting comprises a plurality of constant current sources connected between said sample node and a reference voltage and a plurality of switches corresponding to said plurality of constant current sources and respectively coupled in series therewith.

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